# CSCE-312 | Spring 2020 | Project1

## Building Boolean Logic (Gates and Basic Functions)

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| **Phase1: 30 points**  **When: Friday Feb 7  What: Mini-exercises to be completed during the lab session. TA’s will announce then at the beginning of the lab and you are expected to turn-in solutions at the end of lab session.**  **Phase2: 70 points**  **Due Date:** **Submit on eCampus by Friday, Feb 14th, 11:59 PM**  **Grading**   1. **Project Demo [70%]:** **Demo logistics will be posted on Slack on #Project1 channel** You will be graded for correctness of the chips (hdl) you have designed and coded. You will be running **live** test of all your HDL codes downloaded from your eCampus using Nand2tetris software (Hardware Simulator) with TA. So, make sure to test and verify your codes before finally submitting on eCampus.   ***Rubric:***Each chip needs to pass all its test cases to get full credit, else you will receive a **0 point** on that chip.   1. **Code Review [30%]: To be held with the LIVE Demo** Code review of randomly selected chips. You will be asked to walk through select portions of your code. Also you may be quizzed on circuit diagram of randomly selected chips or truth table.   **Deliverables & Submission**  You need to turn in **the completed HDL files** for **all the chips** implemented. In addition, you need to turn in the completed **tst and cmp files** for the **Xnor and 8-to-3 priority encoder** chips. Put your **full name** in the introductory comment present in each HDL code. Use relevant code comments and indentation. Also, include this **cover sheet** with your signature below. Zip all the required HDL files and the signed cover sheet into a compressed file ***FirstName-LastName-UIN.zip*** . Submit this zip file on eCampus.  **Late Submission Policy:** Refer to the Syllabus |

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| **Full Name: Asa Hayes Section: 503 UIN: 525003952**  **Any assignment turned in without a fully completed cover page will NOT BE GRADED.**  Please list all below all sources (people, books, web pages, etc) consulted regarding this assignment:  CSCE 312 Students Other People Printed Material Web Material (URL) Other  1. 1. Section 503 TA’s1. 1. https://www.electronics-tutorials.ws/combination/comb\_4.html  2. 2. 2. 2. 2.  3. 3. 3. 3. 3.  Please consult the Aggie Honor System Office for additional information regarding academic misconduct – it is your responsibility to understand what constitutes academic misconduct and to ensure that you do not commit it.  I certify that I have listed above all the sources that I consulted regarding this assignment, and that I have not received nor given any assistance that is contrary to the letter or the spirit of the collaboration guidelines for this assignment.  **eCampus Submission Date:** \_\_15 February 2020\_\_\_\_  **Printed Name (in lieu of a signature):** \_\_\_\_Asa Hayes\_\_\_\_\_\_ |